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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,443	11/19/2003	Nicolae Marin	24317/82751	9833

7590 02/01/2005

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EXAMINER	
RILEY, SHAWN	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,443	MARIN ET AL.	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-26 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,4-6 and 8-26 is/are rejected.

7)☒ Claim(s) 2-3 and 7 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant(s) is(are) reminded of the proper content of an abstract of the disclosure.

The abstract should not refer to purported merits (has high power supply ripple rejection ratio) or speculative applications of the invention and should not compare the invention with the prior art (the reference circuit has low speading among similarly manufactured systems. .. .). Correction is required.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-6, 8-12 and 17-25 are rejected under 35 U.S.C. §102(b) as being fully anticipated by Mercer (U.S. Patent 6,198,266). Mercer shows,[1] (in, e.g., the(ir) figures 2a and 2b and corresponding disclosure)

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1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material

As to claim 1;

A band-gap reference circuit (see, e.g., figure 2(a), comprising: a core reference circuit (30), having a core output terminal; a voltage amplifier (Q3 and Q4 and 32), coupled to the core output terminal and having a voltage amplifier terminal; a transconductance amplifier (34), coupled to the voltage amplifier terminal; and a shared voltage rail (see, e.g., Figure 2(b) and Vin), coupled to the core reference circuit and the transconductance amplifier.

As to claim 4;

The reference circuit of claim 1, wherein: the voltage amplifier comprises as input stage, comprising a third transistor(Q4), the third transistor comprising: a third emitter (Q4's emitter coupled through the base to I4) coupled to the ground; and a third base, coupled to core output terminal (between nodes R4 and Q6).

As to claim 5;

The reference circuit of claim 4, wherein the reference circuit is operable to generate a voltage-rail voltage essentially independent of the temperature (as stated in the detailed description at column 4 lines 9-21, the band-gap core comprises a pair of bipolar transistors Q11, Q21 which generate a voltage proportional to absolute temperature (PTAT). A network of resistors connected to these transistors Q11,Q21 are arranged to multiply the PTAT voltage and add it to the base-emitter of one of the transistors so that the total voltage is constant over temperature.)

As to claim 6;

The reference circuit of claim 1, wherein the voltage amplifer comprises more than one stages (the stages include, e.g., in figure 2(b), a differential inputs stage as well as Q3/Q4).

As to claim 8;

The reference circuit of claim 1, wherein the transconductance amplifier comprises more than one stages (M10/M9 and Q5B/Q5A and M8/M7).

As to claim 9;

The reference circuit of claim 1, wherein the reference circuit is powered by a voltage source (Vin) and a current source (I1), coupled in series with the voltage source, wherein the serially coupled voltage source and current source are coupled between the ground and the voltage rail.

As to claim 10;

The reference circuit of claim 1, comprising an output terminal coupled to the voltage rail (coupled through the, in e.g., figure 2(a) the node between 20 and Vout).

11. The reference circuit of claim 1, wherein the reference circuit comprises transistors selected from the group on npn bipolar transistors, pnp bipolar transistors, NMOS, PMOS, CMOS, and BiCMOS transistors.

As to claim 12;

The reference circuit of claim 1, wherein the voltage amplifier and the transconductance amplifier comprise bipolar transistors as first stages (for the voltage amplifier Q1/Q4 and the tranconductance Q5A/Q5B), thereby keeping the noise of the reference circuit below a predetermined level.

As to claim 17;

The reference circuit of claim 1, wherein a ripple rejection ratio is essentially determined by a product of a transconductance of the transconductance amplifier and a voltage gain of the voltage amplifier (by definition, this is how a transconductance amplifier operates vis a vis the voltage gain of an input, e.g., a voltage amplifier).

As to claim 18;

The reference circuit of claim 1, wherein the transconductance amplifier introduces a negative feedback (easiest to see, e.g., in figure 2(a) where output of 34-transconductance amplifier- is fed back to 30-reference circuit) to the reference circuit and the voltage amplifier introduces a positive feedback (see, e.g., figure 2(b) where output of Q4 is connected in a positive feedback configuration to the reference circuit via C1) to the reference circuit, and the magnitude of the negative feedback is bigger than the magnitude of the positive feedback.

As to claim 19;

The reference circuit of claim 1, wherein the reference circuit does not contain a start-up circuit (no startup circuit is described in Mercer).

As to claim 20;

The reference circuit of claim 1, wherein the reference circuit does not contain differential amplifiers (in, e.g., figure 2(b), the reference circuit does not contain a differential amplifier).

As to claim 21;

The reference circuit of claim 1, wherein the spread of the reference circuit is below a predetermined value, wherein the spread comprises the spread of the parameters of similarly manufactured reference circuits (spread of reference circuit is below a predetermined value).

For method claims 22-25, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus will not be repeated.

22. The method of providing a band-gap voltage with a high ripple rejection ratio, the method comprising: providing a core reference circuit, having a core output terminal; providing a voltage amplifier, coupled to the core output terminal and having a voltage amplifier terminal; providing a transconductance amplifier, coupled to the voltage amplifier terminal; providing a shared voltage rail, coupled to the core reference circuit and the transconductance amplifier; and selecting a transconductance of the transconductance amplifier and a voltage gain of the voltage amplifier so that their product generates a band-gap voltage with a ripple rejection ratio in the shared voltage rail above a predetermined value.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole

would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 13-16, and 23-25, are rejected under 35 U.S.C. § 103 as being unpatentable over Mercer (U.S. Patent 6,198,266). The Mercer reference discloses the limitations of the invention as claimed as described above. However, Mercer does not show a supply voltage in a certain range or a specific ripple rejection level in a specific range. It would have been obvious at the time the invention was made to utilize a supply voltage in a certain range or a specific ripple rejection level in a specific range into the circuit of Mercer since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Allowable Subject Matter

5. Claim 2, 3, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

7. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed reference circuit including the claimed circuitry and further the transconductance amplifier coupled to the voltage rail, wherein the coupling of the collector is one of a direct coupling and a coupling across a resistor.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed reference circuit including the claimed circuitry and further the second emitter coupled to the ground, and a second base, coupled to the first base; and a first resistor, coupled between the second collector and the voltage rail, wherein the core output terminal is coupled between the second collector and the first resistor; and said couplings are configured as one of a direct coupling and a coupling across a resistor.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is

found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

January 05

Shawn Riley
Primary Examiner